IN THE SPECIFICATION:

Please replace the following paragraphs:

[0002] In all analog circuit designs it is desirable to have a ground that is as close to 0 volts AC as possible. Normally circuit design assumes that ground nodes do not carry any AC-voltage. If a ground node, contrary to this assumption, does carry an AC-voltage, this may lead to unpredictable behavior, e.g. increased noise, distortion or even instability. The root cause of this is that all conductors have a non-zero impedance. This means that when a ground node has to source or sink a current there will be a voltage drop between the ground node and the actual ground point. This effect is much more pronounced in RF-circuits because the inductive nature of the impedance.

[0003] In integrated circuits the ground point of the die (semiconductor chip) is connected to the exterior via a bonding wire connected between the die and the interposer (or leadframe). The impedance of the bonding wire is important at RF-frequencies, and this makes it difficult to realize a proper ground node on the die. If the die is made bigger in order to make the bonding wire shorter, this only moves the problem from the bonding wire to the die because the conductor on the die has to be longer.

[0004] Several solutions have been proposed to solve this problem. One is to make the C-package very small and the bonding wires short. This solution has several drawbacks. It is only viable for small scale integration circuits. In large scale

integration circuits the die is larger and the ground conductors on the die are correspondingly longer. Moreover for small scale integrated circuits making the bonding wires short only reduces the problem, but does not solve it.

[0009] In general terms according to the present invention the problem is solved by placing a metal-covered area on the interposer under the die. Vias on the interposer connect the area to the underside of the interposer. The die is glued to the area with electrically conducting glue. A capacitor is thus formed, the capacitor being formed by the die substrate, the oxide layer on the underside of the die, and the conductive plate on the interposer. By making all other associated impedances as small as possible, e.g. by connecting the metal-plate on the top side of the interposer to the bottom side by using multiple vias in parallel, the resulting impedance can be made very low, less than 20 Ohms, even at high frequencies. If the integrated circuit has a well defined working frequency, the RF-ground plane can be tuned to that frequency by choosing the dimensions of the associated conductors, and thus the inductance of the conductors, so that the resonant frequency of the inductance and capacitor coincides with the working frequency. The impedance at said working frequency can be made extremely low, close to 2 Ohms.

[0017] The chip I is glued to an insulating interposer 4 carrying a conductive area 5. Typically the conductive area 5 is a metal covered area. The glue 3 is electrically conductive and serves not only the purpose of adhering the chip 1 to the

interposer 4, but also forms a capacitor plate, capacitively coupled to internal parts (not shown) of the chip, but insulated therefrom by the insulating layer 2.

[0020] In this respect it should be noted that even though the metal coated area in the embodiments shown corresponds largely to the dimensions of the chip this is not a prerequisite for the invention to work. Instead, because the electrically conductive glue defines the capacitor plate vis-à-vis the internal parts, it is in principle sufficient to contact the glue 3 to the vias 7.

[0023] The capacitance value has been found to be approximately ten times higher when using electrically conductive glue as compared to non-conductive glue.

[0024] Thus without the electrically conductive glue 3 the capacitance value becomes both smaller and less predictable.

[0028] It is known that any conducting member exhibits an inductance. Thus, a LC series circuit is formed by the capacitance provided between internal parts of the chip and the conductive glue 3 separated by the dielectric layer 2, and the inductance provided by the vias 7. If the chip has a well defined working frequency, the number of vias may be chosen, so that the series resonant frequency of the inductance provided by the vias and the aforementioned capacitance, approximately matches the working frequency of the chip. In this way an extremely low ground impedance of 2 Ohms or less, can be achieved.